CMOS LSI

LC864266A, 864265A

8-bit Single Chip Microcontroller

Overview

The LC864266A/65A microcontrollers are 8-bit single chip microcontrollers with the following on-chip functional blocks:

- CPU : Operable at a minimum bus cycle time of 0.5 μs
- On-chip program ROM maximum capacity : 64 Kbytes
- On-chip look up table ROM maximum capacity :
  64 Kbytes for LC864266A
  32 Kbytes for LC864265A
- On-chip RAM capacity : 512 bytes
- CRT display RAM : 640 × 9 bits
- Closed-caption TV controller and the on-screen display
  controller
- 16-bit timer/counter
- 4-channel × 5-bit AD converter
- 8-bit synchronous serial-interface circuit
- Closed-caption data slicer
- 11-source 9-vectored interrupt system

All of the above functions are fabricated on a single chip.

Package Dimensions

unit : mm

3128-DIP52S

[LC864266A, 864265A]

SANYO : DIP52S
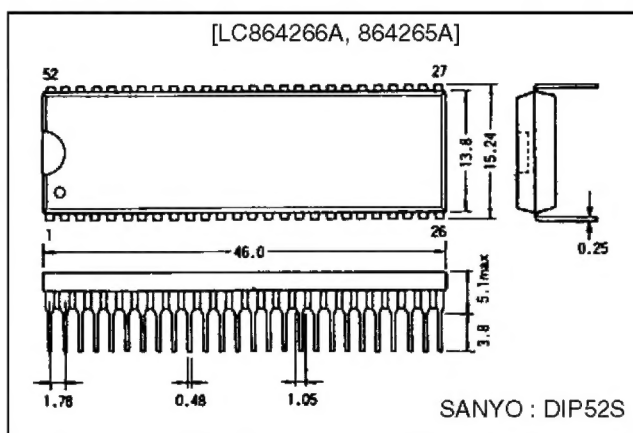
Features

(1) Read-only program memory (ROM) :

	LC864266A	65280 × 8 bits
	LC864265A	65280 × 8 bits

(2) Read-only look up table memory (ROM) :

	LC864266A	65536 × 8 bits
	LC864265A	32768 × 8 bits

(3) Random access memory (RAM) :   512 × 8 bits
640 × 9 bits (for CRT display)

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(4) OSD functions
- Screen for display   : 34 columns × 16 rows (standard character size)
- Display for RAM   : 640 × 9 bits (6 columns for control + 34 columns for display) × 16 rows × 9 bits
- 377 kinds of user specified characters
  - Caption/Text mode   : (9 × 9 dots) × 125 kinds
  - OSD mode   : (12 × 18 dots) × 127 characters (127 characters can also be used in Caption/Text mode)
- Various character attributes
  - Character colors   : 16 colors
  - Character background colors   : 16 colors
  - Fringe / shadow colors   : 16 colors
  - Full screen colors   : 16 colors
  - Fringe / shadow
  - Rounding
  - Underline
  - Italic character (slanting)
- Close-character attribute data changing available
- Vertical display start line setting in row units available (Row overlapping available)
- Horizontal display start position available
- Display mode specification by row (Display mode mixable)
  - caption mode / text mode / OSD mode
- Eight kinds of character size
  - Horiz. × Vert. = (1 × 1), (1 × 2), (2 × 2), (2 × 4)
  - (1.5 × 1), (1.5 × 2), (3 × 2), (3 × 4)
- Shuttering and scrolling in row units available
- Horizontal character pitch selectable : 9 to 16 dots
- Polarity of R, G, B, I, BL output programmable
- Polarity of HS, VS input programmable

(5) Data slicer clock switching function
Clock source is selective from LC oscillation or ceramic resonator (or X'tal) oscillation.

(6) Bus cycle time / Instruction cycle time
The LC864132B/24B/20B/16B/12B microcontrollers are designed to read the ROM twice within one instruction cycle. It has about 1.7 times performance capability within the same instruction-cycle compared to our 4-bit microcontrollers (LC66000 series).
The bus cycle time indicates the speed to read ROM.

Bus cycle time	Instruction cycle time	System clock oscillation	Oscillation frequency	Voltage
0.49 μs	0.99 μs	Ceramic or Crystal	12.08 MHz	4.5 V to 5.5 V
7.5 μs	15.0 μs	Internal RC	800k Hz	4.5 V to 5.5 V

(7) Ports
- Input/output port   : 2 ports (16 lines)
  - Input/output port programmable in nibble unit   : 1 port (8 lines)
  - (When the N-ch open drain output is selected, the data in a bit can be inputted)
  - Input/output port programmable in a bit   : 1 port (8 lines)
- Input port   : 2 ports (8 lines)

(8) A/D converter
-   4-channel × 5-bit AD converter (converted with program)

(9) PWM output
-   10-channel × 7-bit PWM

(10) Timer
-   Timer 0 : 16-bit timer / counter
    2-bit prescaler + 8-bit built-in programmable prescaler
    Mode 0 :   Two 8-bit timers with a programmable prescaler
    Mode 1 :   8-bit timer with a programmable prescaler + 8-bit counter
    Mode 2 :   16-bit timer with a programmable prescaler
    Mode 3 :   16-bit counter
               The resolution of timer is 1 tCYC.
-   Timer 1 : 16-bit timer / PWM
    Mode 0 :   Two 8-bit timers
    Mode 1 :   8-bit timer + 8-bit PWM
    Mode 2 :   16-bit timer
    Mode 3 :   Variable-bit PWM (9 to 16 bits)
               In Mode 0 and Mode 1, the resolution of Timer and PWM is tCYC.
               In Mode 2 and Mode 3, the resolution of Timer and PWM selectable : tCYC or 1/2tCYC by program.

(11) Remote control receiver circuit (shares with the P73/INT3/T0IN terminal)
-   Noise rejection function
-   Polarity switching

(12) Watchdog timer
External RC circuit is required
Interrupt or system reset is selectable

(13) Interrupts
-   11-source 9-vectored interrupts
    1. External Interrupt INT0
    2. External Interrupt INT1
    3. External Interrupt INT2, Timer/counter T0L (Lower 8 bits)
    4. External Interrupt INT3
    5. Timer/counter T0H (Upper 8 bits)
    6. Timer T1H, T1L
    7. Serial interface 0 (SIO0)
    8. Data slicer
    9. Vertical synchronous signal interrupt ($\overline{\text{VS}}$)

-   Interrupt priority control available
    Three interrupt priorities are supported (low, high and the highest) and multilevel nesting is possible. Low or high priority can be assigned to the interrupts from 3 to 10 listed above. For the external interrupt INT0 and INT1, high or the highest priority can be set.

(14) Sub-routine stack level
-   A maximum of 128 levels (Sets the stack inside a RAM.)

(15) Multiplication/division instruction
- 16 bits × 8 bits (7 instruction cycle times)
- 16 bits / 8 bits (7 instruction cycle times)

(16) Three oscillation circuits
- On-chip RC oscillation circuit for the system clock
- On-chip ceramic resonator oscillation circuit for the system clock
- On-chip LC oscillation circuit for the CRT synchronization

(17) Standby function
- HALT mode function
  The HALT mode is used to reduce the power dissipation. In this operation mode, the program execution is stopped.
  This mode can be released by the interrupt request signals or the system reset.
- HOLD mode
  The HOLD mode is used to stop oscillations ; the RC (internal) and the ceramic oscillations.
  This mode can be released by the following conditions.
  • Pull the reset terminal ($\overline{\text{RES}}$) to low level.
  • Feed the selected level to either P70/INT0 or P71/INT1.
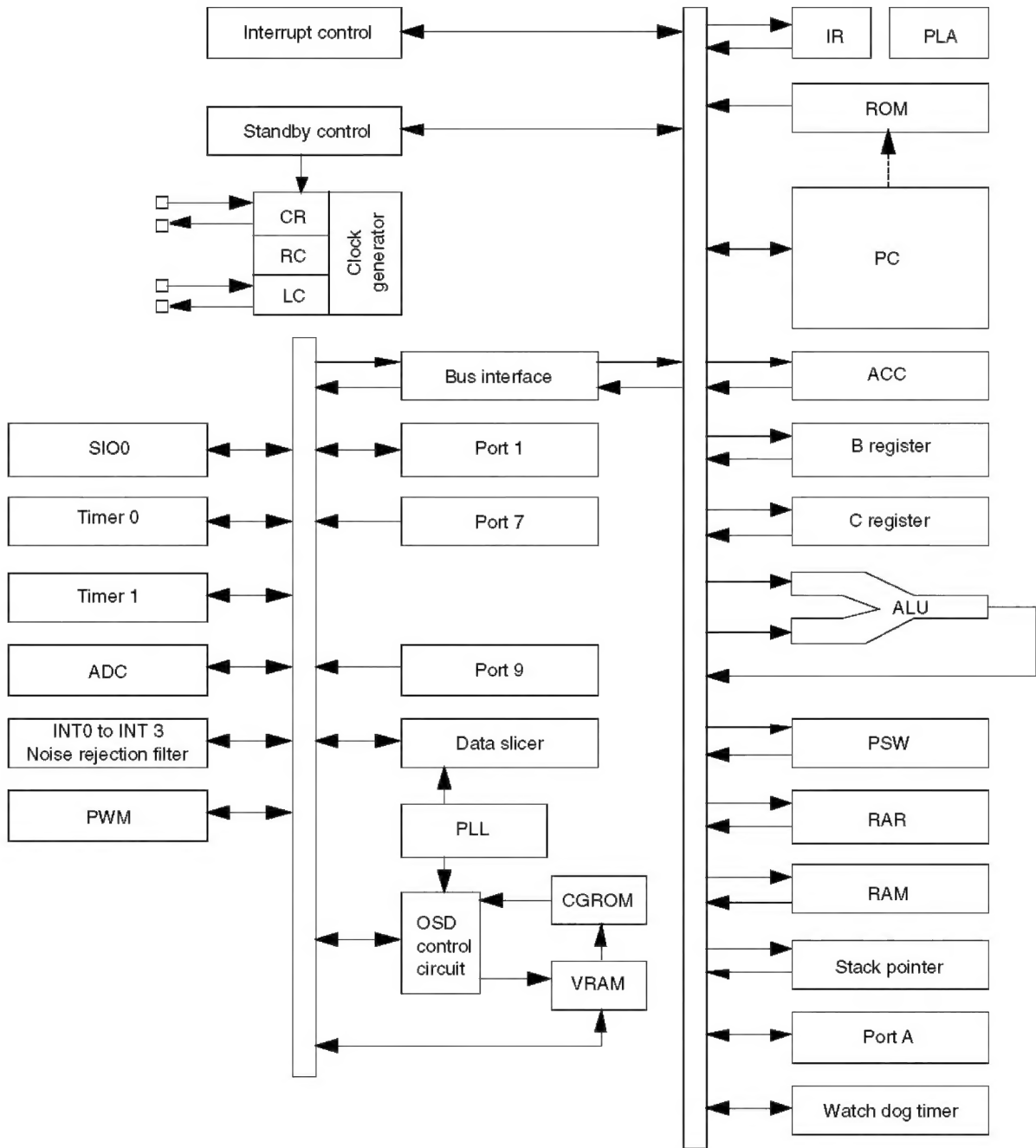
(18) Factory shipment
  DIP52S

(19) Development Tools
- Evaluation (EVA) chip   :   LC866098
- EPROM attached a window   :   LC86E4266
- Emulator   :   EVA86000 (Main) + ECB864200 (Evaluation board) + POD864100 (Pod)

System Block Diagram

Pin Assignment

P10/SO0	1	52	PA7
P11/SI0/SB0	2	51	PA6
P12/SCK0	3	50	PA5
P13	4	49	PA4
P14	5	48	PA3
P15	6	47	PA2
P16	7	46	PA1
P17/PWM	8	45	PA0
DVSS	9	44	P73/INT3/T0IN
CF1	10	43	P72/INT2/T0IN
CF2	11	42	P71/INT1
DVDD	12	41	P70/INT0
P90/AN0	13	40	PWM9
P91/AN1	14	39	PWM8
P92/AN2	15	38	PWM7
P93/AN3	16	37	PWM6
$\overline{RES}$	17	36	PWM5
LC1	18	35	PWM4
LC2	19	34	PWM3
FILT	20	33	PWM2
AVDD	21	32	PWM1
AVSS	22	31	PWM0
CVIN	23	30	BL
$\overline{VS}$	24	29	B
$\overline{HS}$	25	28	G
I	26	27	R

Top view

Pin Description

• Port option can be specified in bit units except the pull-up resistor selection of port 0.

Pin Description Table

Pin name	Pin No.	I/O	Function description	Option
DVSS	9	—	Negative power supply for digital circuit	
CF1	10	Input	Input terminal for ceramic resonator	
CF2	11	Output	Output terminal for ceramic resonator	
DVDD	12	—	Positive power supply for digital circuit	
$\overline{\text{RES}}$	17	Input	Reset terminal	
LC1	18	Input	LC oscillation circuit input terminal	
LC2	19	Output	LC oscillation circuit output terminal	
FILT	20	Output	Filter terminal for PLL	
AVDD	21	—	Positive power supply for analog circuit	
AVSS	22	—	Negative power supply for analog circuit	
CVIN	23	Input	Video signal input terminal	
$\overline{\text{VS}}$	24	Input	Vertical synchronization signal input terminal	
$\overline{\text{HS}}$	25	Input	Horizontal synchronization signal input terminal	
I	26	Output	Image intensity output	
R	27	Output	Red (R) output terminal of RGB image output	
G	28	Output	Green (G) output terminal of RGB image output	
B	29	Output	Blue (B) output terminal of RGB image output	
BL	30	Ouptut	Fast blanking control signal Switch TV image signal and caption/OSD image signal	
PWM0 to PWM9	31 to 40	Output	PWM0 to 9 output terminal 15 V withstand	
Port 1 P10 to P17	1 to 8	I/O	8-bit Input/output port Input/output can be specified in bit units. Other function P10 SIO0 data output P11 SIO0 data input / bus input/output P12 SIO0 clock input/output P17 Timer 1 (PWM) output	Output Format CMOS/Nch-OD (in bit units)
Port 7 P70 P71 to P73	41 42 to 44	I/O Input	4-bit input port Other function P70 INT0 input/HOLD release input/ Nch-transistor output for watchdog timer P71 INT1 input/HOLD release input P72 INT2 input/timer 0 event input P73 INT3 input (noise rejection filter attached input/ timer 0 event input)	Pull-up resistor provided/ not provided (in bit units)

Interrupt receiver formats / vector addresses

	Rising	Falling	Rising/falling	H level	L level	Vector
INT0	enable	enable	disable	enable	enable	03H
INT1	enable	enable	disable	enable	enable	0BH
INT2	enable	enable	enable	disable	disable	13H
INT3	enable	enable	enable	disable	disable	1BH

Continued from preceding page.

Pin name	Pin No.	I/O	Function Description	Option
Port9			4-bit input port	
P90 to P93	13 to 16	Input	Other functions AD converter input port (4 lines)	
Port A			8-bit Input/output port	
PA0 to PA7	45 to 52	I/O	Input/output can be specified in nibble units	

- Any port option can be selected in bit units.
- Port 0 portion   : Pull-up resistor is provided when CMOS output is selected.
                        The pull-up resister is not provided when N-ch Open Drain is selected.
- Port 1 option   : Programmable pull-up resister is provided when any output form is selected.

- Port status during reset

Terminal	I/O	Pull-up resistor status at selecting pull-up option
Port 1	Input	Programmable pull-up resistor OFF
Port 7	Input	Fixed pull-up resistor provided

- AVDD and AVSS are the power supply terminals for built-in analog circuit, while DVDD and DVSS are for built-in digital circuit. Connect them like the following figure to reduce the mutual noise-influence.
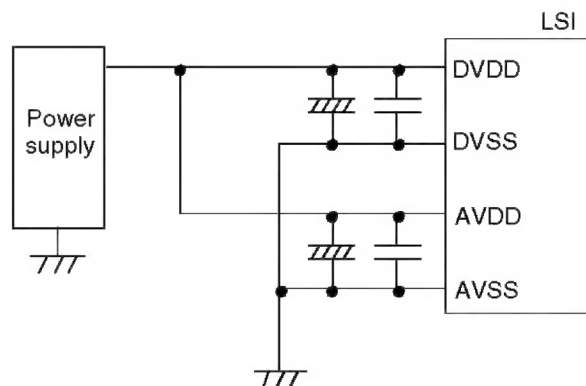
Specifications

1. Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter		Symbol	Pins	Conditions	V_{DD} [V]	Ratings min	typ	max	Unit
Supply voltage		V_{DD}max	DVDD, AVDD	DVDD = AVDD		−0.3		7.0	V
Input voltage		$V_I(1)$	• P71, 72, 73 • Port 9 • $\overline{RES}$, $\overline{HS}$, $\overline{VS}$, CVIN			−0.3		V_{DD}+0.3	
Output voltage		$V_O(1)$	R, G, B, BL, I, FILT			−0.3		V_{DD}+0.3	
		$V_O(2)$	PWM0 to PWM9			−0.3		15	
Input/output voltage		V_{IO}	Ports A, 1, P70			−0.3		V_{DD}+0.3	
High-level output current	Peak output current	$I_{OPH}(1)$	Ports A, 1	• Pull-up MOS transistor output • At each pin		−2			mA
		$I_{OPH}(2)$	Ports A, 1	• CMOS output • At each pin		−4			
		$I_{OPH}(3)$	R, G, B, BL, I	• CMOS output • At each pin		−5			
	Total output current	$\Sigma I_{OAH}(1)$	Port 1	The total of all pins		−10			
		$\Sigma I_{OAH}(2)$	Port A	The total of all pins		−10			
		$\Sigma I_{OAH}(3)$	R, G, B, BL, I	The total of all pins		−15			
Low-level output current	Peak output current	$I_{OPL}(1)$	Ports A, 1	At each pin				20	
		$I_{OPL}(2)$	P70	At each pin				30	
		$I_{OPL}(3)$	• R, G, B, BL, I • PWM0 to PWM9	At each pin				5	
	Total output current	$\Sigma I_{OAL}(1)$	Port A	The total of all pins				40	
		$\Sigma I_{OAL}(2)$	Port 1, P70	The total of all pins				40	
		$\Sigma I_{OAL}(3)$	R, G, B, BL, I	The total of all pins				15	
		$\Sigma I_{OAL}(4)$	PWM0 to PWM9	The total of all pins				30	
Maximum power dissipation		Pd max	DIP52S	Ta = −30 to +70°C				430	mW
Operating temperature range		Topr				−30		+70	°C
Storage temperature range		Tstg				−55		+125	

* DVSS and AVSS must be supplied the same voltage, V_{SS}. V_{SS} = DVSS = AVSS
DVDD and AVDD must be supplied the same voltage, V_{DD}. V_{DD} = DVDD = AVDD

2. Recommended Operating Range at Ta = –30°C to +70°C, V$_{SS}$ = 0 V

Parameter	Symbol	Pins	Conditions	V$_{DD}$ [V]	Ratings			Unit
					min	typ	max	
Operating supply voltage range	V$_{DD}$	DVDD, AVDD	0.98 μs ≤ tCYC tCYC ≤ 1.02 μs		4.5		5.5	V
Hold voltage	V$_{HD}$	DVDD, AVDD	RAMs and the registers hold data at HOLD mode.		2.0		5.5	
Input high voltage	V$_{IH}$(1)	Port A (Schmitt)	Output disable	4.5 to 5.5	0.6V$_{DD}$		V$_{DD}$	
	V$_{IH}$(2)	• Port 1 (Schmitt) • P72, 73 • HS,VS	Output disable	4.5 to 5.5	0.75V$_{DD}$		V$_{DD}$	
	V$_{IH}$(3)	• P70 port input / interrupt • P71 • RES (Schmitt)	Output N-channel transistor OFF	4.5 to 5.5	0.75V$_{DD}$		V$_{DD}$	
	V$_{IH}$(4)	• P70 Watchdog timer input	Output N-channel transistor OFF	4.5 to 5.5	V$_{DD}$–0.5		V$_{DD}$	
	V$_{IH}$(5)	Port 9 port input		4.5 to 5.5	0.7V$_{DD}$		V$_{DD}$	
Input low voltage	V$_{IL}$(1)	Port A (Schmitt)	Output disable	4.5 to 5.5	V$_{SS}$		0.2V$_{DD}$	
	V$_{IL}$(2)	• Port 1 (Schmitt) • P72, 73 • HS,VS • Port 9	Output disable	4.5 to 5.5	V$_{SS}$		0.25V$_{DD}$	
	V$_{IL}$(3)	• P70 port input / interrupt • P71 • RES (Schmitt)	N-channel transistor OFF	4.5 to 5.5	V$_{SS}$		0.25V$_{DD}$	
	V$_{IL}$(4)	• P70 Watchdog timer input	N-channel transistor OFF	4.5 to 5.5	V$_{SS}$		0.6V$_{DD}$	
	V$_{IL}$(5)	Port 9 port input		4.5 to 5.5	V$_{SS}$		0.3V$_{DD}$	
CVIN input amplitude	V$_{CVIN}$	CVIN		5.0	1Vp-p –3dB	1Vp-p	1Vp-p +3 dB	Vp-p *
Operation cycle time	tCYC(1)		OSD function	4.5 to 5.5	0.97	1	1.02	μs
	tCYC(2)		Except OSD function	4.5 to 5.5	0.97		40	

* Vp-p : Peak-to-peak voltage

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Parameter	Symbol	Pins	Conditions	V_{DD} [V]	min	typ	max	Unit
Oscillation frequency range (Note 1)	FmCF (1)	CF1, CF2	12 MHz (ceramic resonator oscillation) Refer to Figure 1.	4.5 to 5.5	11.76	12	12.24	MHz
	FmCF (2)		12.08 MHz (ceramic resonator oscillation) Refer to Figure 1.		11.84	12.08	12.32	
	FmLC	LC1, LC2	14.11 MHz (LC oscillation) Refer to Figure 2.	4.5 to 5.5		14.11		
	FmRC		RC oscillation	4.5 to 5.5	0.3	0.8	2.0	
Oscillation stable time period (Note 2)	tmsCF (1)	CF1, CF2	12 MHz (ceramic resonator oscillation) Refer to Figure 3.	4.5 to 5.5		0.02	0.2	ms
	tmsCF (2)		12.08 MHz (ceramic resonator oscillation) Refer to Figure 3.			0.02	0.2	

(Note 1) Refer to Table 1 and Table 2 for the oscillation constant.

(Note 2) The oscillation stable time is a period necessary for the oscillation to be stable after the power first applied, the HOLD mode released and the main-clock oscillation stop instruction released.
Refer to the Figure 3 for details.

3. Electrical Characteristics at Ta = –30°C to + 70°C , V$_{SS}$ = 0 V

Parameter	Symbol	Pins	Conditions	Ratings				Unit
				V$_{DD}$ [V]	min	typ	max	
Input high-level current	I$_{IH}$(1)	• Port 1 • Port A	• Output disable • Pull-up MOS transistor OFF • V$_{IN}$ = V$_{DD}$ (including the off-leak current of the output transistor)	4.5 to 5.5			1	µA
	I$_{IH}$(2)	• Port 7 without pull-up MOS transistor • Port 9 • $\overline{RES}$ • $\overline{HS}$,$\overline{VS}$	V$_{IN}$ = V$_{DD}$	4.5 to 5.5			1	
Input low-level current	I$_{IL}$(1)	• Port 1 • Port A	• Output disable • Pull-up MOS transistor OFF • V$_{IN}$ = V$_{SS}$ (including the off-leak current of the output transistor)	4.5 to 5.5	–1			
	I$_{IL}$(2)	• Port 7 without pull-up MOS transistor • Port 9	V$_{IN}$ = V$_{SS}$	4.5 to 5.5	–1			
	I$_{IL}$(3)	• $\overline{RES}$ • $\overline{HS}$,$\overline{VS}$	V$_{IN}$ = V$_{SS}$	4.5 to 5.5	–1			
Output high-level voltage	V$_{OH}$(1)	CMOS output of ports A, 1	I$_{OH}$ = –1.0 mA	4.5 to 5.5	V$_{DD}$–1			V
	V$_{OH}$(2)	R, G, B, BL, I	I$_{OH}$ = –0.1 mA	4.5 to 5.5	V$_{DD}$–0.5			
Output low-level voltage	V$_{OL}$(1)	Ports A, 1	I$_{OL}$ = 10 mA	4.5 to 5.5			1.5	
	V$_{OL}$(2)	Ports A, 1	• I$_{OL}$ = 1.6 mA • The total current of the ports A, 1 is not over 40 mA.	4.5 to 5.5			0.4	
	V$_{OL}$(3)	• R, G, B, BL, I • PWM0 to PWM9	• I$_{OL}$ = 3.0 mA • The current of any unmeasured pins is not over 3 mA.	4.5 to 5.5			0.4	
	V$_{OL}$(4)	P70	I$_{OL}$ = 1 mA	4.5 to 5.5			0.4	
Pull-up MOS transistor resistance	Rpu	• Ports A, 1 • Port 7	V$_{OH}$ = 0.9V$_{DD}$	4.5 to 5.5	13	38	80	kΩ
Output off-leakage current	I$_{OFF}$	PWM0 to PWM9	V$_{OUT}$ = 13.5 V	4.5 to 5.5			5	µA
Hysteresis voltage	V$_{HIS}$	• Ports A, 1 • Port 7 • $\overline{RES}$ • $\overline{HS}$,$\overline{VS}$	Output disable	4.5 to 5.5		0.1V$_{DD}$		V

Parameter	Symbol	Pins	Conditions	Ratings				Unit
				V$_{DD}$ [V]	min	typ	max	
Input clamp voltage	V$_{CLMP}$	CVIN		5.0	2.3	2.5	2.7	V
Pin capacitance	CP	All pins	• f = 1 MHz • Unmeasured input pins are set to V$_{SS}$ level. • Ta = 25°C	4.5 to 5.5		10		pF

4. Serial Input/Output Characteristics at Ta = –30°C to +70°C , V$_{SS}$ = 0 V

Parameter			Symbol	Pins	Conditions	Ratings				Unit
						V$_{DD}$ [V]	min	typ	max	
Serial clock	Input clock	Cycle	tCKCY(1)	• SCK0 • SCLK0	Refer to Figure 5.	4.5 to 5.5	2			tCYC
		Low-level pulse width	tCKL(1)			4.5 to 5.5	1			
		High-level pulse width	tCKH(1)			4.5 to 5.5	1			
	Output clock	Cycle	tCKCY(2)	• SCK0 • SCLK0	• Use an external pull-up resistor (1 kΩ) during open drain output • Refer to Figure 5.	4.5 to 5.5	2			
		Low-level pulse width	tCKL(2)			4.5 to 5.5		1/2tCKCY		
		High-level pulse width	tCKH(2)			4.5 to 5.5		1/2tCKCY		
Serial input	Data set-up time		tICK	• SI0	• Data set-up to SCK0 rising	4.5 to 5.5	0.1			μs
	Data hold time		tCKI		• Data hold from SCK0 rising • Refer to Figure 5.	4.5 to 5.5	0.1			
Serial output	Output delay time (External serial clock)		tCKO(1)	• SO0	• Use an external pull-up resistor (1 kΩ) during open drain output.	4.5 to 5.5			7/12tCYC +0.2	μs
	Output delay time (Internal serial clock)		tCKO(2)		• Data set-up to SCK0 falling • Data hold from SCK0 falling • Refer to Figure 5.	4.5 to 5.5			1/3tCYC +0.2	

5. Pulse Input Conditions at Ta = –30°C to +70°C, V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions		Ratings			Unit
				V_{DD} [V]	min	typ	max	
High/low-level pulse width	tPIH(1) tPIL(1)	• INT0, INT1 • INT2/T0IN	• Interrupt acceptable • Timer/counter 0 pulse countable	4.5 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3/T0IN (The noise rejection clock is selected to 1/1)	• Interrupt acceptable • Timer/counter 0 pulse countable	4.5 to 5.5	2			
	tPIH(3) tPIL(3)	INT3/T0IN (The noise rejection clock is selected to 1/16)	• Interrupt acceptable • Timer/counter 0 pulse countable	4.5 to 5.5	32			
	tPIL(4)	$\overline{RES}$	Reset acceptable	4.5 to 5.5	200			µs
	tPIH(5) tPIL(5)	$\overline{HS}$, $\overline{VS}$	Display position controllable Each active edge of $\overline{HS}$, $\overline{VS}$ must be more than 1tCYC. Refer to Figure 7.	4.5 to 5.5	10			tCYC
Rising/falling time	tTHL tTLH	$\overline{HS}$	Refer to Figure 7.	4.5 to 5.5			500	ns
Horizontal pull-in range	FH	$\overline{HS}$	The monitor point in Figure 10 is 1/2 V_{DD}.	4.5 to 5.5	15.23	15.73	16.23	kHz

6. A/D Converter Characteristics at Ta = –30°C to +70°C, V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions		Ratings			Unit
				V_{DD} [V]	min	typ	max	
Resolution	N			4.5 to 5.5		5		bit
Absolute precision	ET		(Note 3)	4.5 to 5.5		±1/4	±3/4	LSB
Conversion time	tCAD	From selecting Vref to resulting	1 bit conversion time = 2tCYC	4.5 to 5.5			1.96	µs
Reference current	I_{REF}		(Regulate the ladder resistor)	4.5 to 5.5		1.0	2.0	mA
Analog input voltage range	V_{AIN}	AN0 to AN3		4.5 to 5.5	V_{SS}		V_{DD}	V
Analog port input current	I_{AINH}		$V_{AIN} = V_{DD}$	4.5 to 5.5			1	µA
	I_{AINL}		$V_{AIN} = V_{SS}$	4.5 to 5.5	–1			

(Note 3)   Absolute precision excepts quantizing error (±1/2 LSB).

7. Current Drain Characteristics at Ta = –30°C to +70°C , V_{SS} = 0 V

Parameter	Symbol	Pins	Conditions		Ratings			Unit
				V_{DD} [V]	min	typ	max	
Current drain during basic operation (Note 4)	$I_{DDOP}(1)$	DVDD, AVDD	• FmCF = 12 MHz Ceramic resonator oscillation • FmLC = 14.11 MHz LC oscillation • System clock : CF oscillation • Internal RC oscillation stops	4.5 to 5.5		21	32	mA
Current drain in HALT mode (Note 4)	$I_{DDHALT}(1)$	DVDD, AVDD	• HALT mode • FmCF = 12 MHz or 12.08 MHz Ceramic resonator oscillation • FmLC = 0 Hz (oscillation stops) • System clock : CF oscillation • Internal RC oscillation stops.	4.5 to 5.5		5	10	mA
	$I_{DDHALT}(2)$	DVDD, AVDD	• HALT mode • FmCF = 0 MHz (oscillation stops) • FmLC = 0 Hz (oscillation stops) • System clock : Internal RC	4.5 to 5.5		300	800	µA
Current drain in HOLD mode (Note 4)	I_{DDHOLD}	DVDD, AVDD	• HOLD mode • All oscillation stops.	4.5 to 5.5		0.05	20	µA

(Note 4)　The currents of the output transistors and the pull-up MOS transistors are ignored.

Oscillation type	Manufacturer	Oscillator	C1	C2
12 MHz ceramic resonator oscillation	Murata	CSA12.0MTZ	33 pF	33 pF
		CST12.0MTW	on chip	
	Kyocera	KBR-12.0M	33 pF	33 pF
12.08 MHz ceramic resonator oscillation	Murata	CSA 12.0MTZ021	33 pF	33 pF
	Kyocera	KBR-12.08M	33 pF	33 pF

* Both C1 and C2 must use an K rank (±10%) and an SL characteristics.

Table 1. Ceramic Resonator Oscillation Guaranteed Constant (Main-clock)

Oscillation	L	C3	C4
14.11 MHz LC oscillation	4.7 μH	33 pF	45 pF (Trimmer)
	4.7 μH±10% (Variable)	33 pF	33 pF

* See Figure 11, 12 for LC oscillation characteristics.

Table 2. LC Oscillation Guaranteed Constant (OSD clock)

(Notes) • Since the circuit pattern affects the oscillation frequency, place the oscillation-related parts as close to the oscillation pins as possible with the shortest pattern length.
 • If you use other oscillators than those shown above, we provide no guarantee for the characteristics.
 • Adjust the voltage of monitor point in figure 10 to $1/2 \ V_{DD}\pm10\%$ by the LC oscillation constant 'L' or 'C' to lock the PLL circuit.
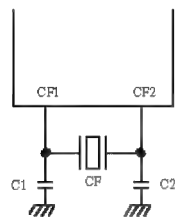
Main clock

Figure 1   Ceramic Resonator Oscillation
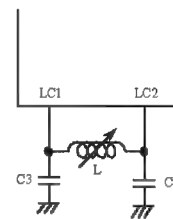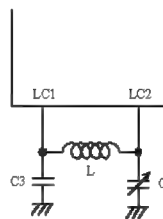
OSD clock

Figure 2   LC Resonator Oscillation 1, 2
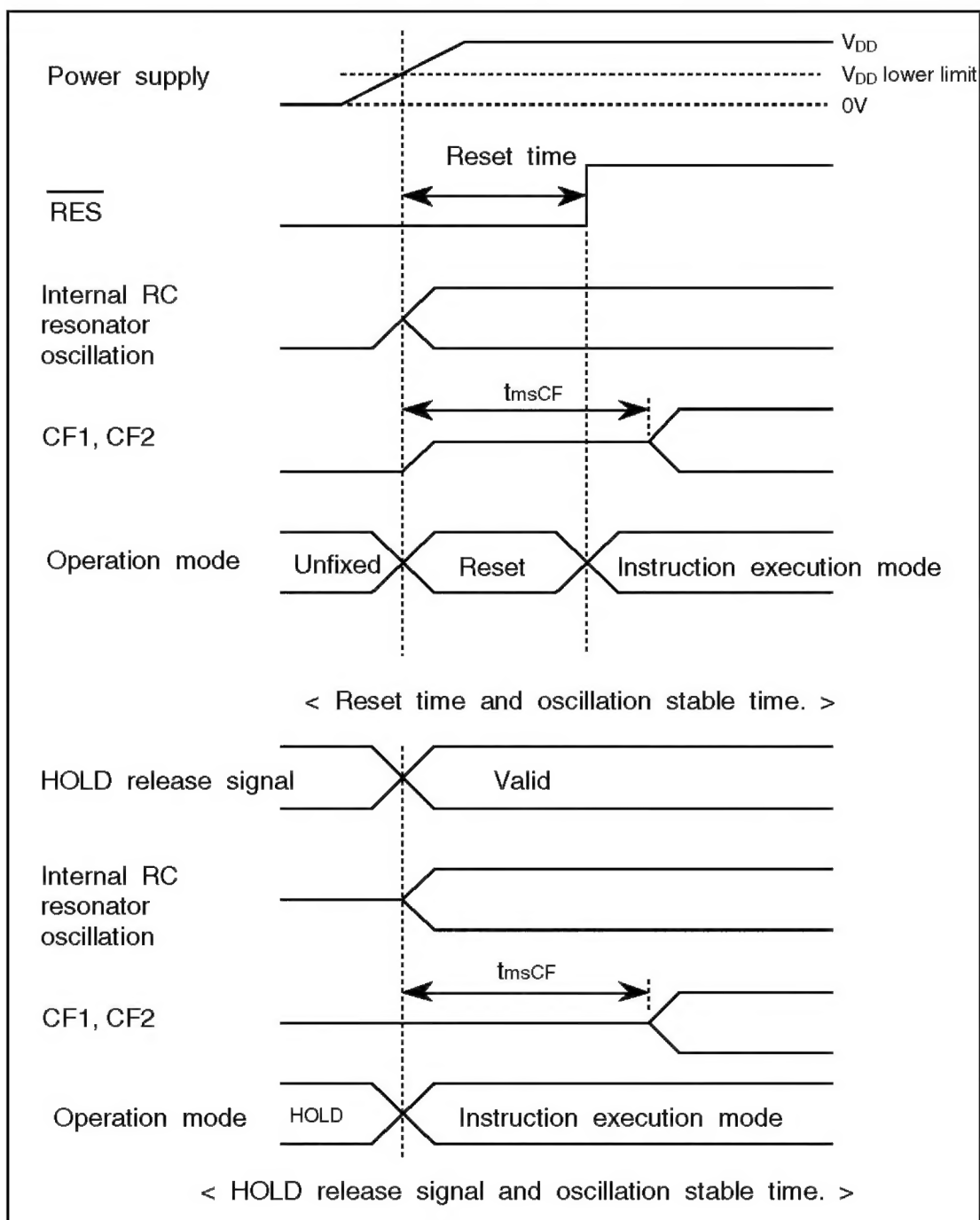
Figure 3 Oscillation Stable Time

(Note) Set the values of C_{RES}, R_{RES} so that the reset time is 200 μs or longer.

Figure 4 Reset Circuit

< AC timing point >

< Timing >

< Test load >
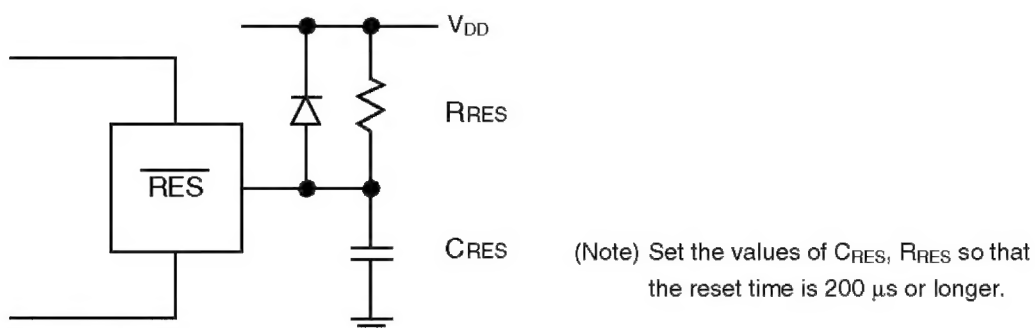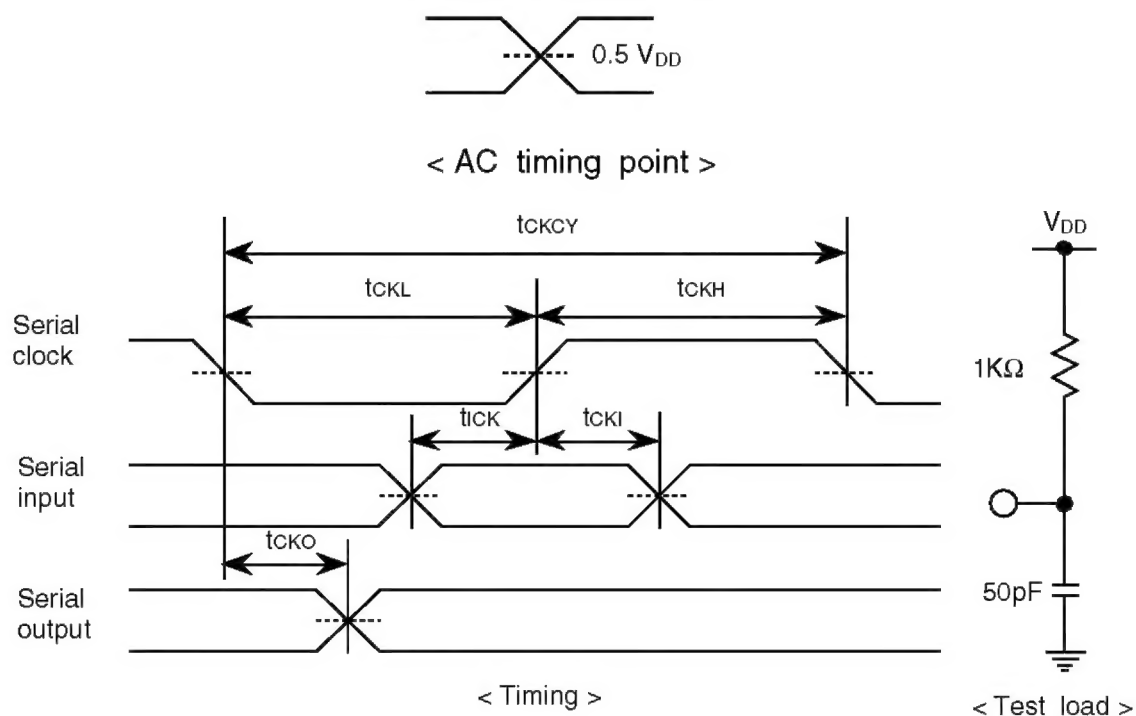
Figure 5 Serial Input/output Test Condition
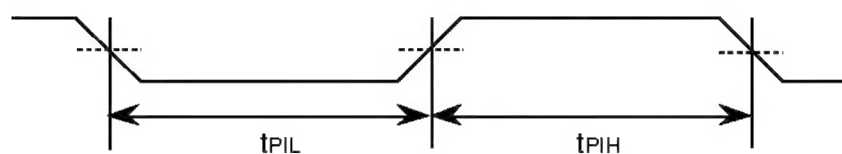
Figure 6 Pulse Input Timing Condition - 1

(a) In case of active low

(b) In case of active high
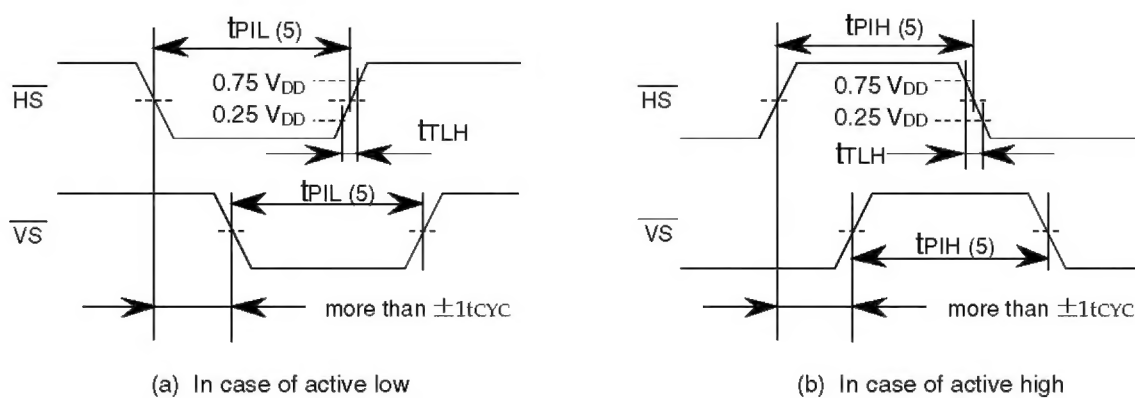
Figure 7 Pulse Input Timing Condition - 2
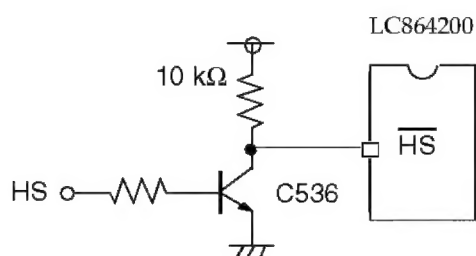
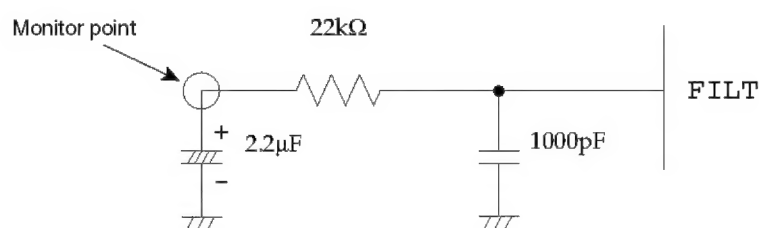Figure 8 Recommended Interface Circuit
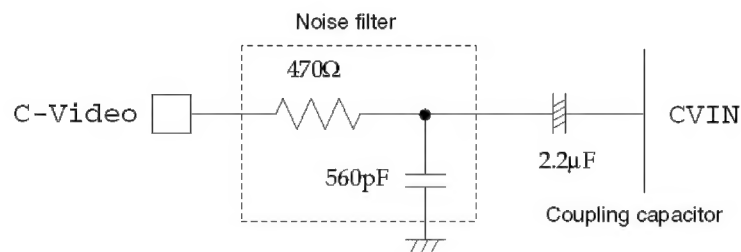
Figure 9   CVIN Recommended Circuit

Figure 10   FILT Recommended Circuit

(Note)   • Place the parts connected FILT terminal as close to the FILT as possible with the pattern length on the board.
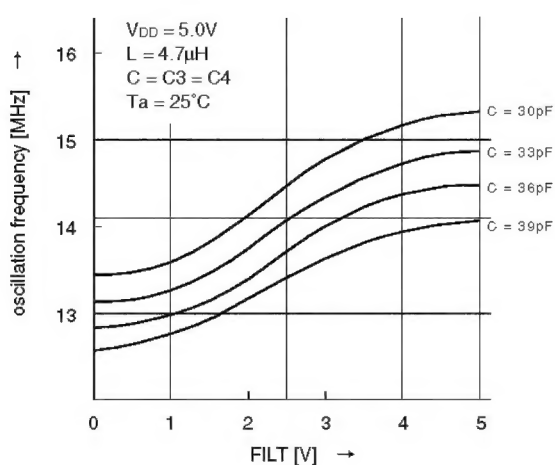
Figure 11 FILT-LC Oscillation Frequency (1)
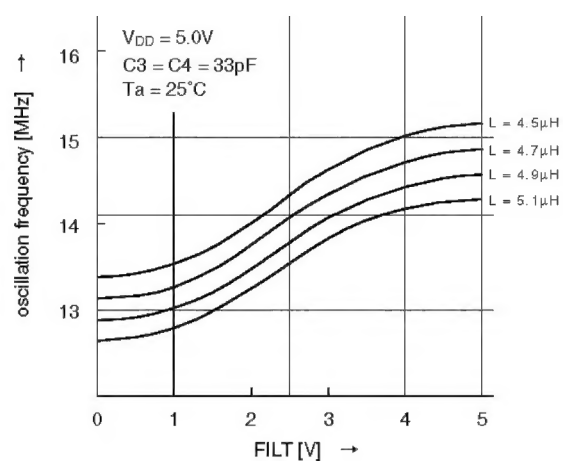
Figure 12 FILT-LC Oscillation Frequency (2)